OCENME

# OSP7N80C / OSF7N80C

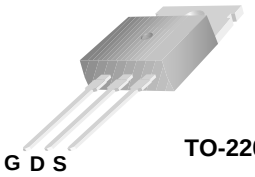
## 800V N-Channel MOSFET

### General Description

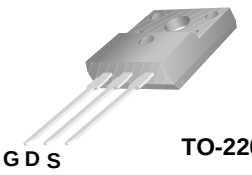
This Power MOSFET is produced using ocenme's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

### Features

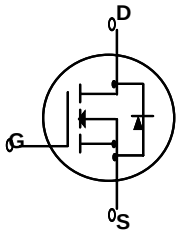
- 7.0A, 800V, $R_{DS(on)}$ = 2.00Ω @$V_{GS}$ = 10 V
- Low gate charge ( typical 30nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability




TO-220




TO-220F




## Absolute Maximum Ratings

$T_C$ = 25°Cunless otherwise noted

| Symbol | Parameter | | OSP7N80C | OSF7N80C | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 800 | | V |
| $I_D$ | Drain Current - Continuous ($T_C$ = 25°C) | | 7.0 | 7.0* | A |
| | - Continuous ($T_C$ = 100°C) | | 4.2 | 4.2 * | A |
| $I_{DM}$ | Drain Current - Pulsed | (Note 1) | 28 | 28* | A |
| $V_{GSS}$ | Gate-Source Voltage | | ± 30 | | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 653 | | mJ |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 16.7 | | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 4.5 | | V/ns |
| $P_D$ | Power Dissipation ($T_C$ = 25°C) | | 167 | 56 | W |
| | - Derate above 25°C | | 1.33 | 0.44 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | | °C |
| $T_L$ | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | 300 | | °C |

* Drain current limited by maximum junction temperature.

## Thermal Characteristics

| Symbol | Parameter | OSP7N80C | OSF7N80C | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 0.75 | 2.25 | °C/W |
| $R_{\theta CS}$ | Thermal Resistance, Case-to-Sink Typ. | 0.5 | -- | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 62.5 | 62.5 | °C/W |

## Electrical Characteristics

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 800 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | -- | 1 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 800 V, $V_{GS}$ = 0 V | -- | -- | 10 | μA |
| | | $V_{DS}$ = 640 V, $T_C$ = 125°C | -- | -- | 100 | μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 30 V, $V_{DS}$ = 0 V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -30 V, $V_{DS}$ = 0 V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 3.0 | -- | 5.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.5 A | -- | 1.6 | 2.0 | Ω |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 1300 | -- | pF |
| $C_{oss}$ | Output Capacitance | | -- | 120 | -- | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 10 | -- | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 400 V, $I_D$ = 7.0A, $R_G$ = 25 Ω (Note 4, 5) | -- | 40 | -- | ns |
| $t_r$ | Turn-On Rise Time | | -- | 100 | -- | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 50 | -- | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 60 | -- | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 640 V, $I_D$ = 7.0 A, $V_{GS}$ = 10 V (Note 4, 5) | -- | 30 | - | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 8.0 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 11.0 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 7.0 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 28 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 7.0 A | -- | -- | 1.5 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_S$ = 7.0 A, $dI_F$ / dt = 100 A/μs (Note 4) | -- | 650 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 7.0 | -- | μC |

**Notes:**
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 25mH, $I_{AS}$ = 7.0 A, $V_{DD}$ = 50V, $R_G$ = 25 Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 7.0 A, di/dt ≤ 200A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

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## Typical Characteristics

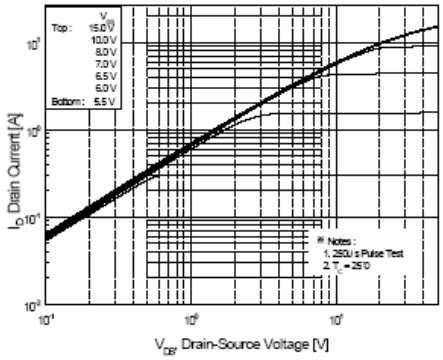



**Figure 1. On-Region Characteristics**

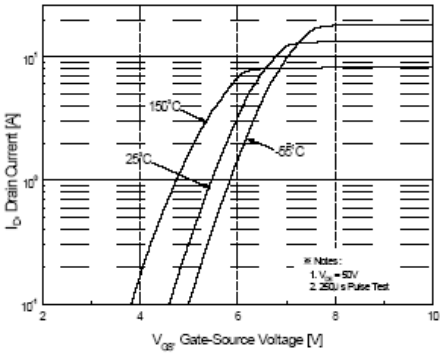



**Figure 2. Transfer Characteristics**

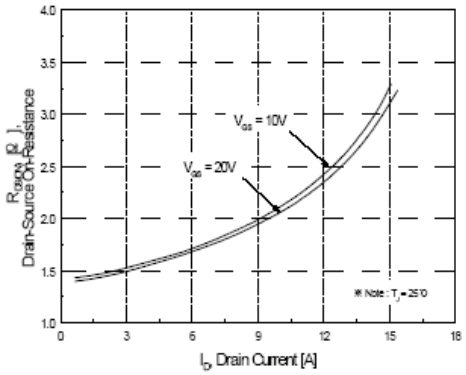



**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**

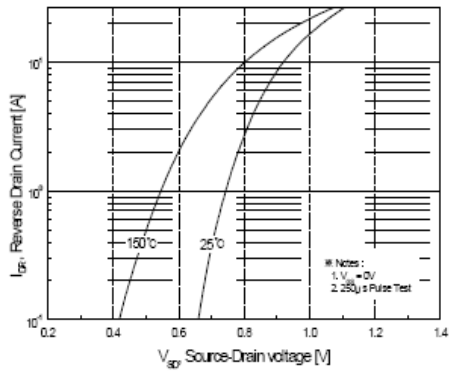



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**

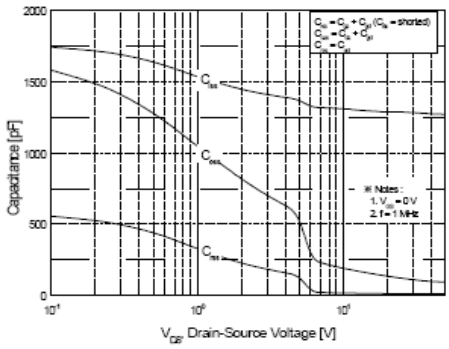



**Figure 5. Capacitance Characteristics**

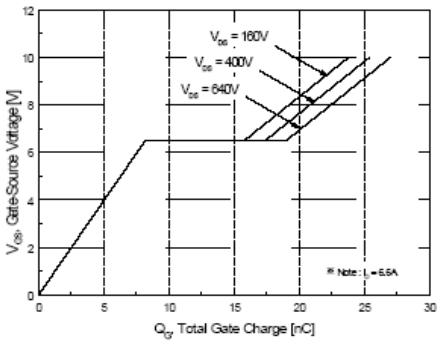



**Figure 6. Gate Charge Characteristics**

## Typical Characteristics (Continued)

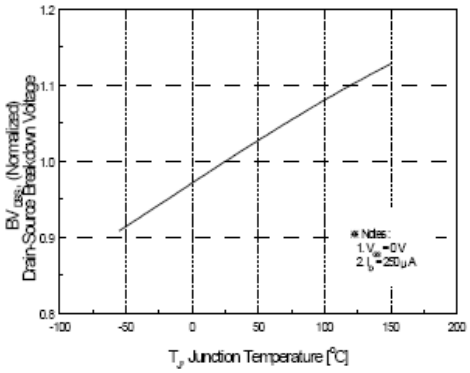



**Figure 7. Breakdown Voltage Variation vs Temperature**

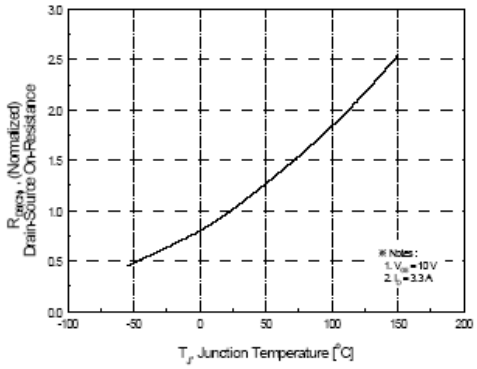



**Figure 8. On-Resistance Variation vs Temperature**

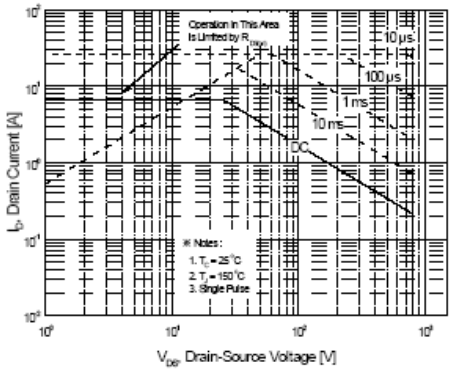



**Figure 9-1. Maximum Safe Operating Area for OSP7N80C**

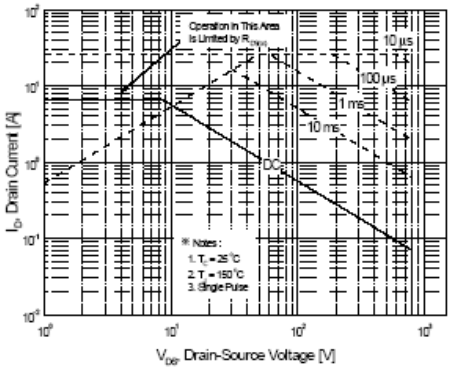



**Figure 9-2. Maximum Safe Operating Area for OSF7N80C**

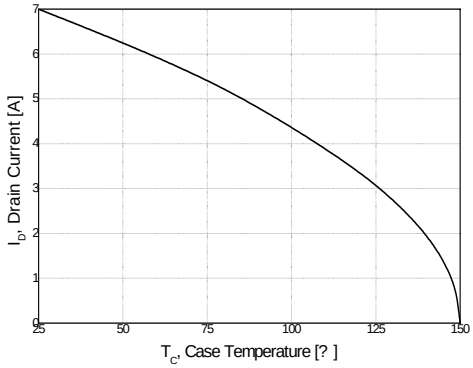



**Figure 10. Maximum Drain Current vs Case Temperature**

# OSP7N80C / OSF7N80C

## Typical Characteristics (Continued)

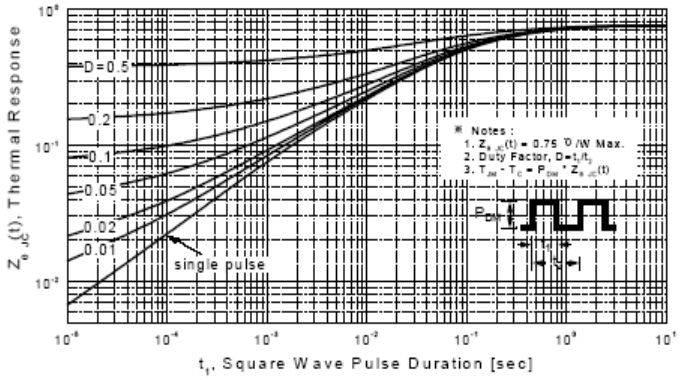



**Figure 11-1. Transient Thermal Response Curve for OSP7N80C**

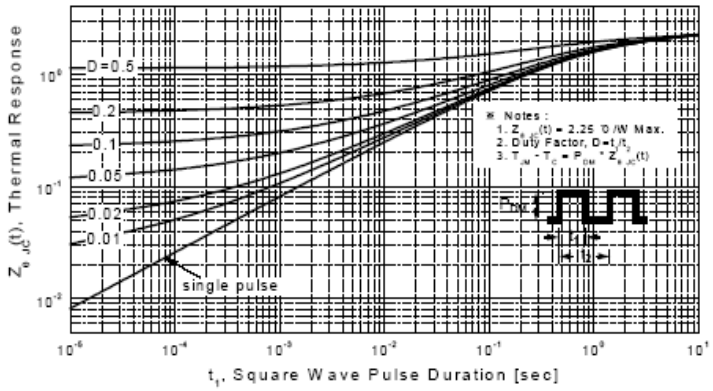
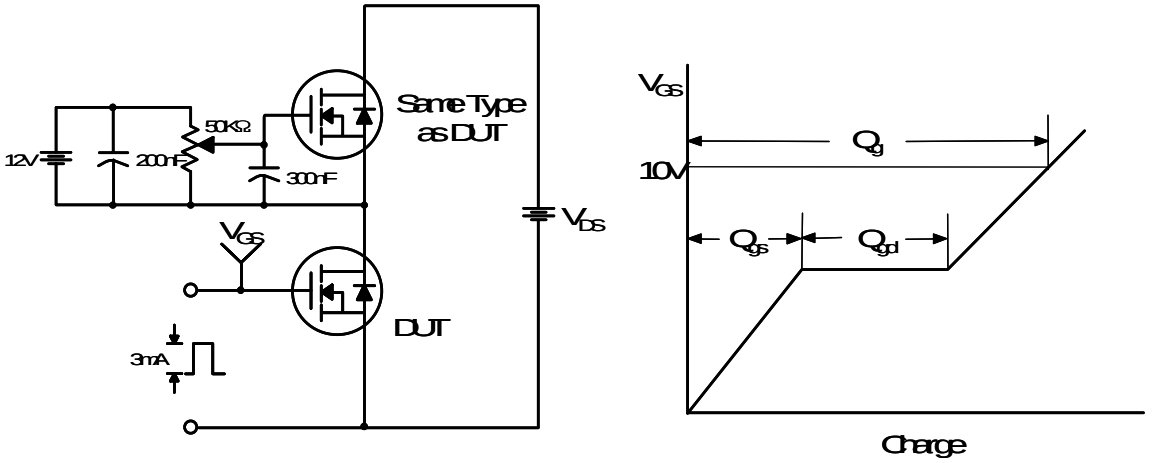
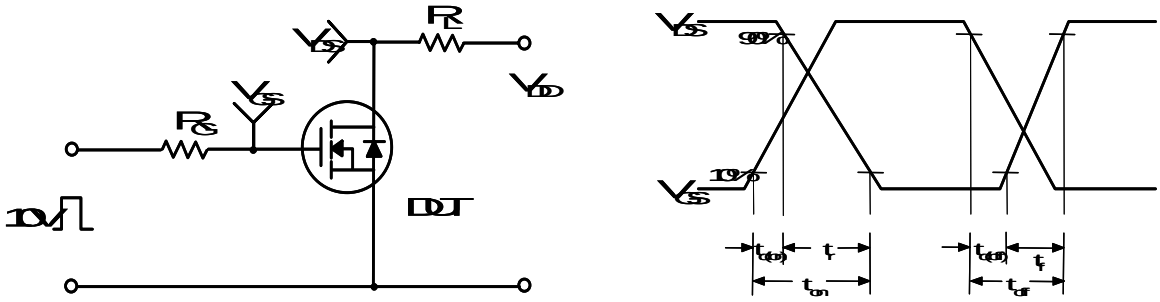



**Figure 11-2. Transient Thermal Response Curve for OSF7N80C**

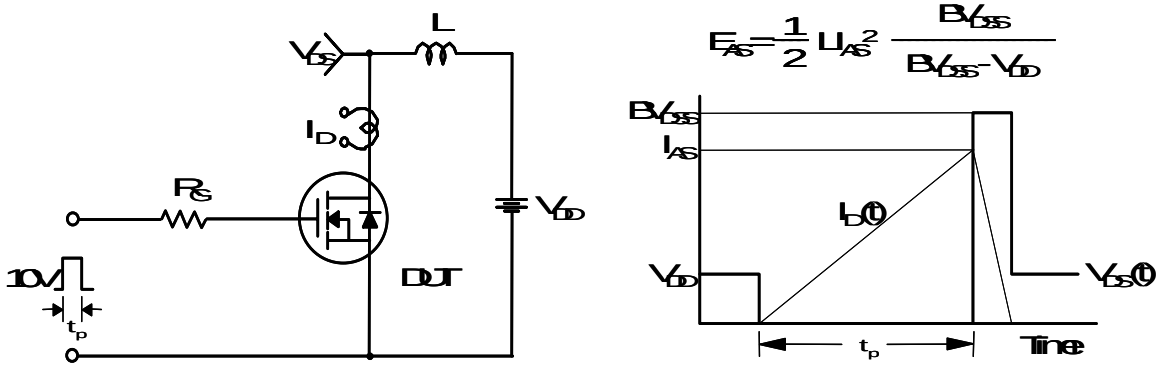
**Gate Charge Test Circuit & Waveform**




**Resistive Switching Test Circuit & Waveforms**




**Unclamped Inductive Switching Test Circuit & Waveforms**



**Peak Diode Recovery dv/dt Test Circuit & Waveforms**